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A Fast Switching Current Controlled DC/DC Converter for Automotive Applications

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Abstract: Automotive industry requires integrated circuits with both low cost, to maintain product competitiveness, and high efficiency, moving towards solutions as green as possible. Each electronic device within the car needs for a regulator to provide a steady supply to ensure correct and safe operation. Among all regulator, DC/DC Converters are the most valid solution to achieve a high efficiency-price ratio. The DC/DC Converter needs for a control loop to monitor the load operation. The basic control loop topologies are well known in the state-of-the-art. The paper presents a DC/DC Buck Converter for automotive applications designed in low cost technology with an upgraded version of the Peak Current Mode Control which uses a constant off-time. For chip area reduction, an n-channel power-DMOS is chosen as power transistor. The design of each block composing the circuit is presented. To guarantee DC-DC Buck converters high-efficiency and low cost (in terms of external components) increasing switching frequency is mandatory. A ≥ 1.5 MHz switching frequency has been chosen to reduce external components size. The device is optimized by design to be able to achieve 94.4% efficiency using a 3V – 3A load. The post-layout simulations of the system are shown, confirming the expected circuit behavior also including the presence of wiring parasites. A PCB is also designed to test the packaged die to ultimately demonstrate the chip's robustness and suitability in a real automotive application.

Keywords: DC/DC Converter, Current Control, Peak Current Mode Control, Constant-Toff

1. Introduction

Nowadays, thanks to their higher efficiency-price ratio, the switching DC/DC converters are covering almost all automotive applications, replacing the conventional converters. To keep the cost of such systems competitive, integrated circuits are required, which integrate external components as much as possible, or which work with smaller external components. A typical application is to drive constant current electronic devices, such as mechanic valves. Each load, or device, must be carefully driven to function correctly: they cannot be connected directly to the car battery, whose voltage might range between 4.5 and 27 V (considering cold cranking), or irreversible damages and failures would result. In fact, a regulator must be placed in the middle that guarantees the load to operate according to its current/voltage specifications. In fact, the car battery sources the regulator that guarantees the application load, e.g. the front light, in a stable manner the desired volt/ampere magnitude [1]. The use of power electronic circuits would require very high voltage conversion ratio, while DC/DC converters, such as the Buck converter, use the high duty cycle to achieve high step-down ratios. Through design optimization, external components can be shrunk and scaled so that their parasitic effects (e.g. from the Equivalent Series Resistor) cause less losses, resulting in a higher overall efficiency. However, inductive DC/DC converters would require large magnetic components (inductors), which cannot be integrated, and with greater parasitic. To improve the situation, the typical frequency of hundreds-kHz can be increased up to 1 MHz. To implement such a high frequency in high-power nodes where very large devices, i.e. large capacitor, are used, an accurate circuit design is essential [2].

To monitor the operation of the load, the DC/DC converter needs a control loop [3]. Among the various solutions, the Peak Current Mode Control (PCMC) is chosen to maintain a

low circuit complexity, linked to costs. However, the basic PCMC is not very reliable: instability issues arise when the duty cycle exceeds 50%, which can occur in a car battery-powered application [4, 5]. A slope compensation technique is usually used to overcome the problem [6, 7]. Instead, the paper presents a PCMC with a Constant off-time, an upgrade which allows to solve instability issues, improving the efficiency of the circuit, without affecting its complexity.

In many DC-DC converters applications there is an external diode to charge the bootstrap capacitor and an external power transistor to supply the load [8, 9]. These external components affect the size of the PCB. To reduce the size of the external components it is necessary to improve the gate driver and level shifter design, therefore minimizing the problems related to the switching speed. In fact, these blocks require the development of new solutions. The paper proposes a way to fully integrate these external components. Indeed, the power transistor and the circuit used to charge the bootstrap capacitor were integrated on silicon, lowering the capacitances, inductances and resistances in the PCB [8]. The goal is to increase the gate driver frequency up to 1 MHz, with high dV/dt for the power transistor V_{DS}. The proposed gate driver, bootstrap circuit and level shifter are designed for a load that requires a constant current of 3 A with an input voltage range between 4.5 V and 27 V.

The paper is organized as follows: the system architecture and the block designs are presented in Section II; the simulation results are reported in Section III and Sections IV draws the conclusions.

2. DC/DC Controlled Buck Converter

The overall architecture of the circuit is shown in Figure 1. The external components needed are the following: the inductor (L), the Schottky Diode and the Bootstrap capacitor. The main blocks, according to the Figure 1, are: the Current Sensing, the Control Logic blocks, the Protection, the Internal Reference (including a bandgap voltage reference to generate *Vmax*, related to *Imax*), the gate Driver to turn the Power-DMOS on and off and the Power Supply to generate a low voltage domain for the low side circuit. The choice of the power-DMOS is based on the switching frequency and losses [10].

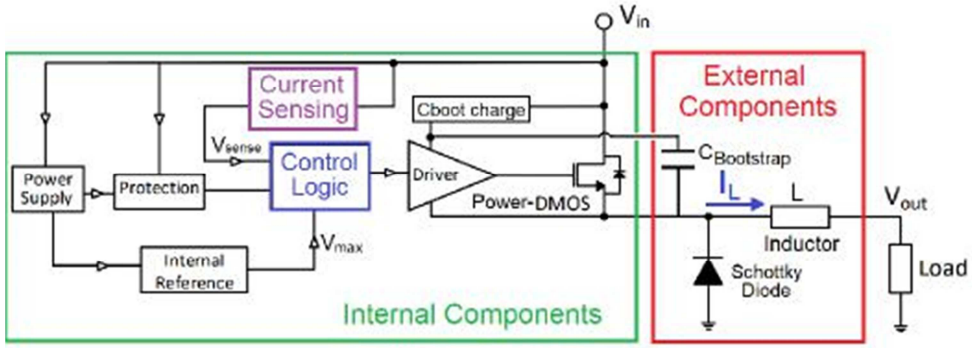

Figure 1. *Top level Schematic.*

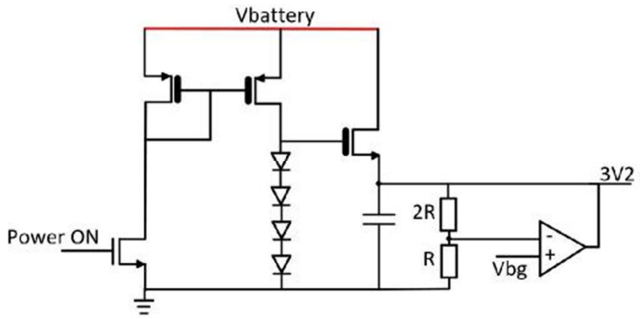

Figure 2. *Power Supply schematic.*

2.1. Power Supply

The power Supply block is sourced by the battery voltage (12V nominal). It is used to provide the low-side low-voltage domain, the source of all other circuits presented below. Figure 2 shows its design. A voltage drop is generated by exploiting a cascade of NMOS diodes. Between the diodes and the battery voltage there is a high side PMOS, which mirrors the current once the power ON is activated and also keeps the two domains separated. A high side NMOS is then used to regulate the output voltage. In particular, through a voltage bandgap *Vbg*, a reference *Vref = 1 V* is created. The power supply output node is maintains the desired voltage using a fed back error amplifier where the inverting input is given by the resistor divider and the non-inverting input by the *Vbg*. In general, for a wide circuit it is preferable to have current references rather than voltage ones. Indeed, long metal would result in voltage drops due to parasitics, affecting the precision. Therefore, all the currents will be generated, then brought where needed and eventually, by letting them flow through some proper resistors, the voltage values are taken back.

2.2. UVLO

Once the voltage source for analog and digital circuits has been generated, the UVLO circuit gives the enable and starts the circuit. As shown in Figure 3, the core of the circuit is a comparator where the negative input is connected to the reference voltage from the power supply, while the positive node voltage comes from a resistor divider R1 and R2 (+R3) where R3 is a switched resistor. At the beginning, the switch is closed and short-circuited to ground. As soon as the supply

grows, the positive node grows and, as a consequence, the comparator output goes up. However, initially, due to a sudden change of state, it will most probably oscillate. Through hysteresis (inverting the comparator output), the switch is opened and, as a result, the comparator positive input sees a resistor divider R1 and R2+R3. This further increases the positive node voltage and stabilizing the comparator output. The signal coming from the comparator output is then squared by using a cascade of a Schmitt trigger and an inverter, to have a digital signal.

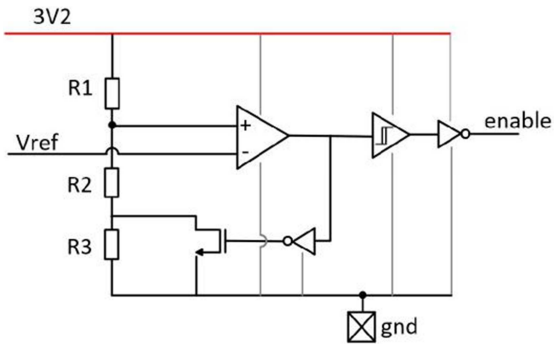

Figure 3. *UVLO schematic.*

The UVLO signal is subsequently delayed. Indeed, it is convenient to wait before enabling the level shifter: the nodes of the circuits otherwise are not uniquely defined and wrong states may occur. Meanwhile, the bootstrap capacitor is charging. The delay is simply achieved by letting a known current flow over a known capacitance, connected only when the UVLO signal is ready. The capacitor voltage provides the input to a Schmitt trigger, which, connected in series to an inverter, produces the desired delayed signal, later used as an enable.

2.3. Control Loop

The control logic is based on the Peak Current Mode Control (PCMC). Among the possible upgrades, a Constant Toff technique was used [11-13]. The goal is to prevent the output current from exceeding a peak reference value. Once the output current reaches the reference, the power-DMOS must be turned off to decrease the current. After *Toff* seconds, the power-DMOS turnes on again. The current will then rise again and the system will continue to operate, resulting in a saw-tooth waveform. To be able to count up to *Toff* seconds, the system needs an oscillator and a counter. The oscillator generates a clock with a given frequency (e.g. 8MHz). As shown in Figure 4, the circuit uses an AND port whose inputs come from the UVLO signal and the oscillator output fed-back. The AND output will either make a PMOS or a NMOS conducting which will either pull up or down the common node. In fact, a current is mirrored in this branch and flows onto a capacitor, giving the input to a Schimtt trigger. An inverter completes the circuit giving both the oscillator output and the feedback for the AND port input. At every cycle, the oscillator output changes. Indeed, at first, the PMOS is conducting, since the UVLO signal is 0. The capacitor is therefore charged and the cascade Schmitt-inverter gives 1. This way, the NMOS starts conducting, the oscillator state changes again and so on. The mirrored current, whose value identifies the Toff value, is externally. Indeed, the greater the current flowing, the faster the capacitor charges, resulting in a higher oscillator frequency and vice versa.

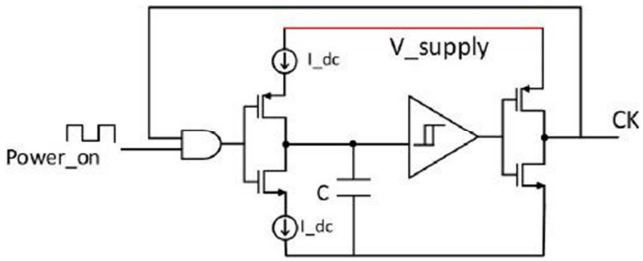

Figure 4. *Oscillator schematic.*

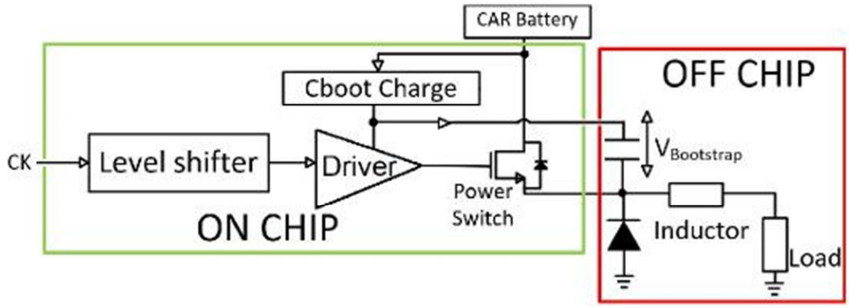

Figure 5. *Gate driver architecture.*

The oscillator signal, CK, acts as an input for the counter. The counter will always count up to the same quantity, but the bit flips slower/faster depending on the chosen oscillator current. The 4-bit counter is designed using four D flip-flops: each clock commutation changes the state of the first flip-flop. Every two commutations, the second flip-flop commutates, etc. The last commutation will therefore be 1111, with a speed given by the mirrored current in the oscillator. A signal is then sent to the gate driver via a SR Latch, indicating that the power-DOMS must be switched on and, in the meantime, the counter is reset.

2.4. Gate Driver

The proposed on-chip HV gate driver architecture is shown in Figure 5 [9, 14]. It consists of: the level shifter, the bootstrap charge and the driver itself [10]. *Vbootstrap* is a floating voltage that can vary from below ground to above

battery voltage. The level shifter moves the low voltage domain (low side) signal to a high voltage domain for the output stage. In fact, the $0 - 3\ V$ signal coming from the counter cannot be used directly to switch on the power-DMOS (for example, if the source is 6 *V,* $3V$ would not be enough). The Gate Driver will be supplied by an external capacitor during its ON phase, called Bootstrap Capacitor and placed as in Figure 5. This is necessary to keep the power transistor on while keeping its source as high as the supply voltage. The bootstrap capacitor connected to DMOS source ensures proper driver supply regardless of the output voltage.

The driver itself eventually turns the power-DMOS on and off. The driver takes the input from the level shifter. Since the power-DMOS gate capacitance, *Cgate*, is quite big, the driver must sink enough current to turn it on quickly (e.g. 10ns). A cascade of inverters is therefore used, where each stage has huger dimensions than the previous one. In this way, each inverter can drive the following one fast enough. The last stage will be designed such that:

$$R_{eq}\, C_{gate} = 10nS \tag{1}$$

where *Req* is the inverter equivalence resistance, approximately 10Ω (high W).

2.5. Current Sensing and SET

An internal Current Sensing technique allows to reduce the components on silicon, resulting in a cheaper solution, shown in Figure 6. The current flows through a sense resistor and its voltage drop is read by a readout circuit. If the voltage drop is higher than the reference, a comparator flips. The comparator reference value can be changed at will, resulting in a different current peak. The comparator output and the delayed sensing trigger signal are used as inputs for an AND port which is used to provide a more steady comparator output after its commutation. Next, the signal is squared and a one-shot is produced. This will disable the high side PMOS when needed. Indeed, when the sense current reaches the *Imax* reference, the comparator commutes and the PMOS switches off. Therefore the output, connected to the SR Latch SET signal, goes from Vbootstrap to ground, switching off the power-DMOS. The power consumption is reduced as the current is now only read during the on-phase (when the power-DMOS conducts), rather than during the entire switching period.

3. Simulations and PCB

The above system was design, layouted and simulated. Here a 1-ohm resistor has been chosen as a load. Figure 7 shows the driver signal which turns the power-DMOS on and off. The output current obtained, with saw-tooth shape, is shown in Figure 8. The circuit settings are the following: *Ipeak* of 1.7 A and a frequency of 900 kHz. By changing the references (the oscillator current and the current sensing comparator current), the system can be pushed to operate up to 3 A peak and 1.8 MHz, as proven in Figure 9. With a 1 ohm resistor, however, only a 2.8A peak current was reached.

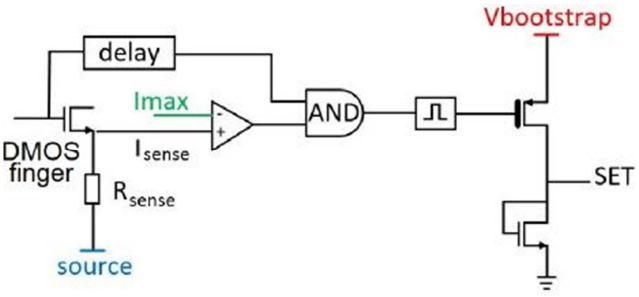

Figure 6. *Current Sensing technique.*

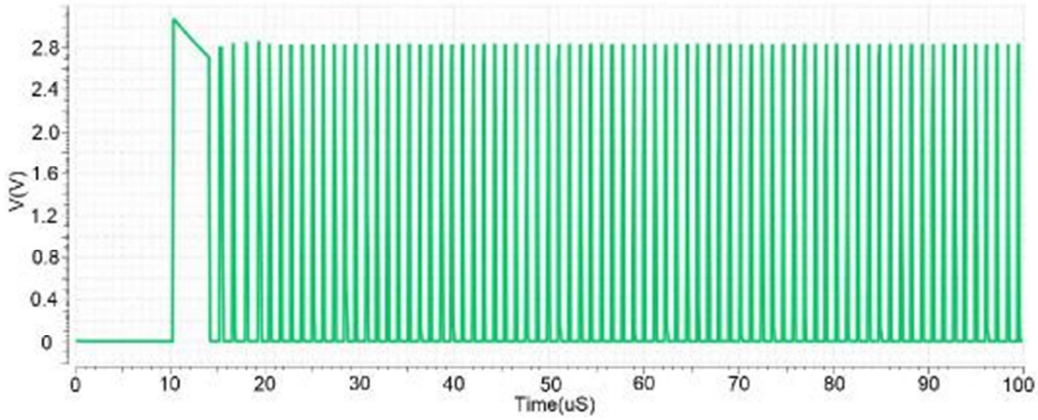

Figure 7. *Power-DMOS Vgs.*

In the meantime, a PCB has been designed. Figure 10 shows the Constant Toff PCB. In particular, at the top right a potentiometer will vary the resistance and therefore will modify the two reference currents. In this way it is possible to test the functioning of the system by varying both the *Toff* time and the *Ipeak* value and compare it with the results obtained in the previous simulations.

4. Conclusion

The paper outlines the analog design of an integrated current-controlled DC/DC Buck Converter for automotive battery powered applications. The overall circuit has been divided into blocks, each of which performs a crucial function.

The transistor level concept of these blocks was presented. The DC/DC Converter designed here achieves an efficiency of 94.4% when driving a *4.5 V – 3 A* load with a maximum switching frequencyof *1 MHz*. The simulation results proved that the whole system works as expected. The circuit was layouted and sent to fabrication for the production of silicon wafer. Next, the corresponding wafer reticle will be plastic-packaged to be soldered on the PCB. The laboratory test will conclude the research, ultimately demonstrating whether the chip can reliably and solidly drive a true automotive application load as resulted from software simulations. Future challenges will further improve the presented topology by leveraging upcoming even more efficient power transistor technology to achieve higher switching frequencies for even higher load control.

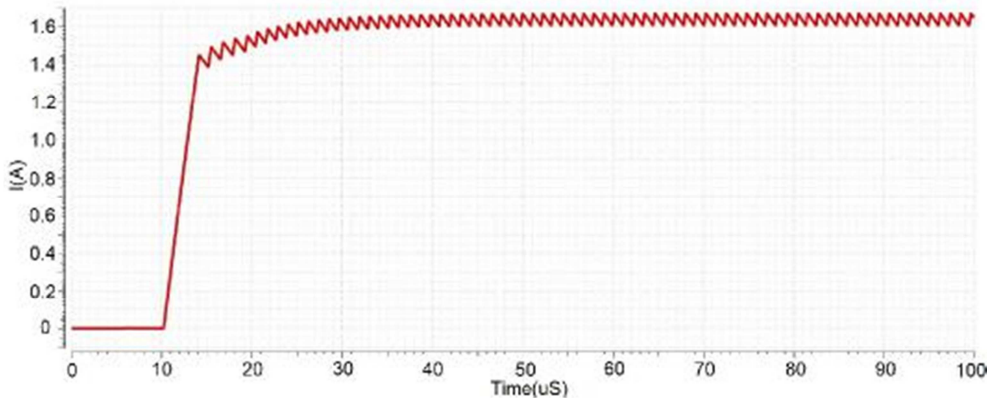

Figure 8. *DC/DC Converter simulation, nominal operation.*

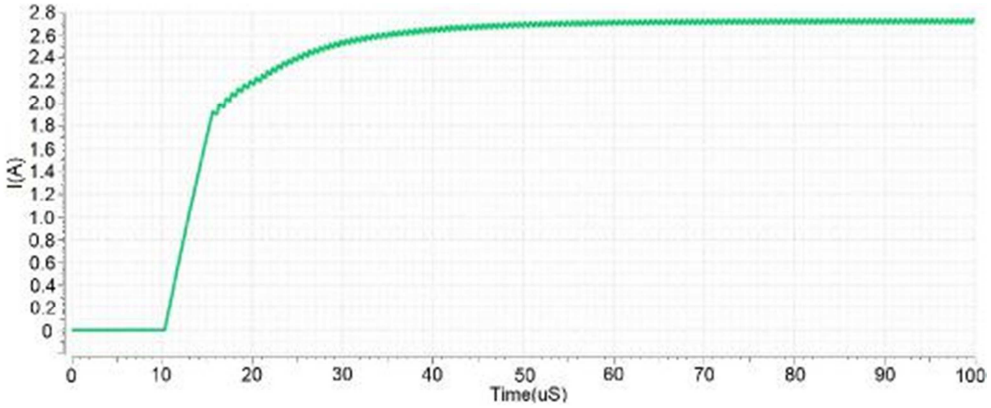

Figure 9. *DC/DC Converter simulation, high performance.*

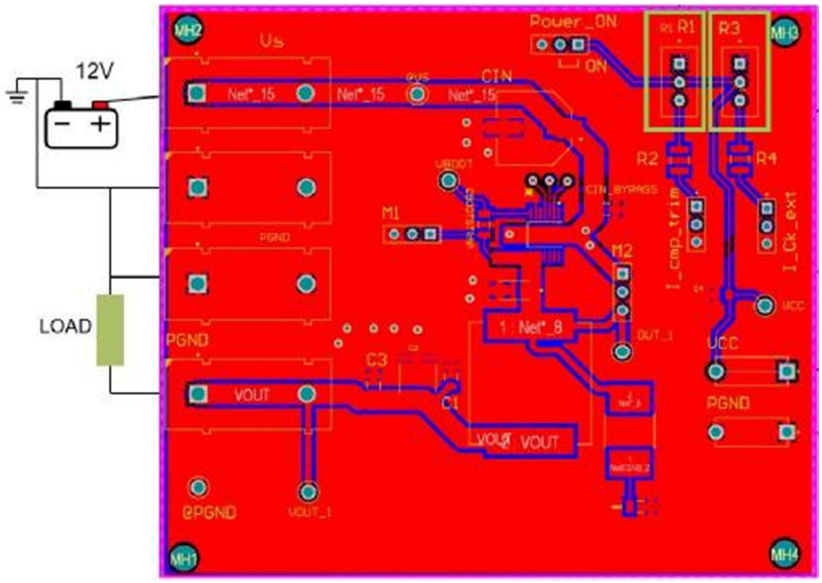

Figure 10. *DC/DC Converter PCB.*

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The data that support the findings of this study are available from the corresponding author, O. G., upon reasonable request.

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